EE303B Fall 2017

**Report on Lab#2**

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**Part I. Design and Simulation of 1-bit Adder with gate delay**

**1. Design of 1-bit Adder**

a. The truth table of 1-bit adder is given as the following table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Cin | B | A | S | Cout |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

b. The above truth table can be implemented using 2-input based carry source generation and propagation method:

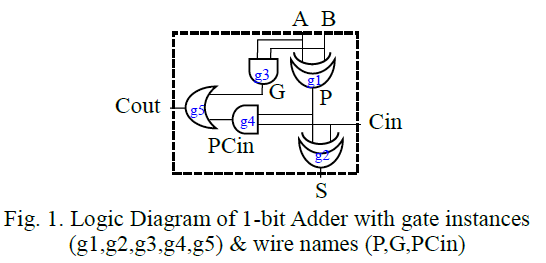
b-1) The truth table of carry generation and propagation, G and B, for two inputs, A and B, can be done as follows:

|  |  |  |
| --- | --- | --- |
| AB | G (carry generation) | P (carry propagation) |
| 00 | 0 | 0 |
| 01 | 0 | 1 |
| 10 | 0 | 1 |
| 11 | 1 | 0 |

The related logic equations are:

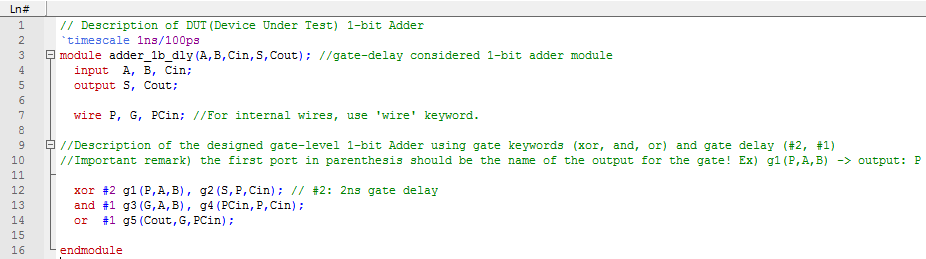
G = A & B, P = A ^ B

b-2) The gate implementation of 1-bit adder using G and P can be done as follows:

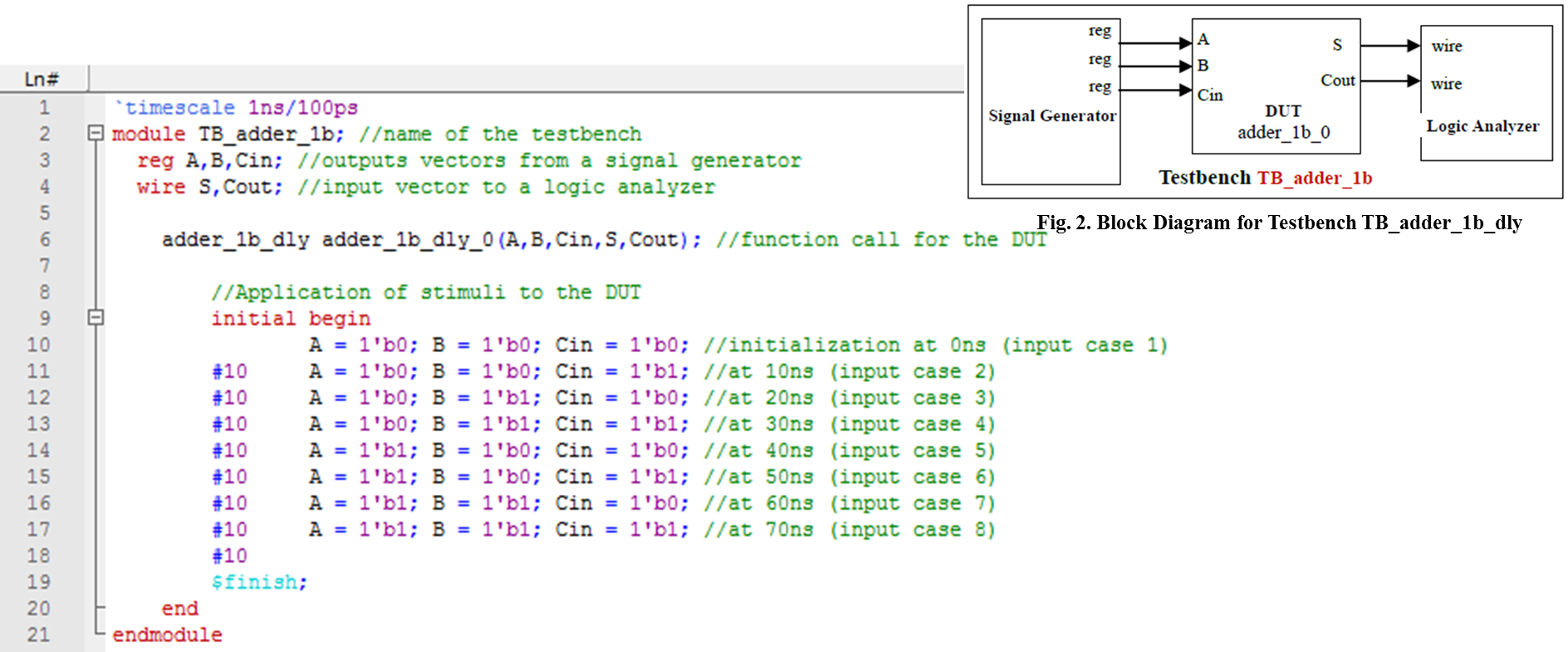


**2. Simulation**

1) Coding of DUT (1-bit Adder)

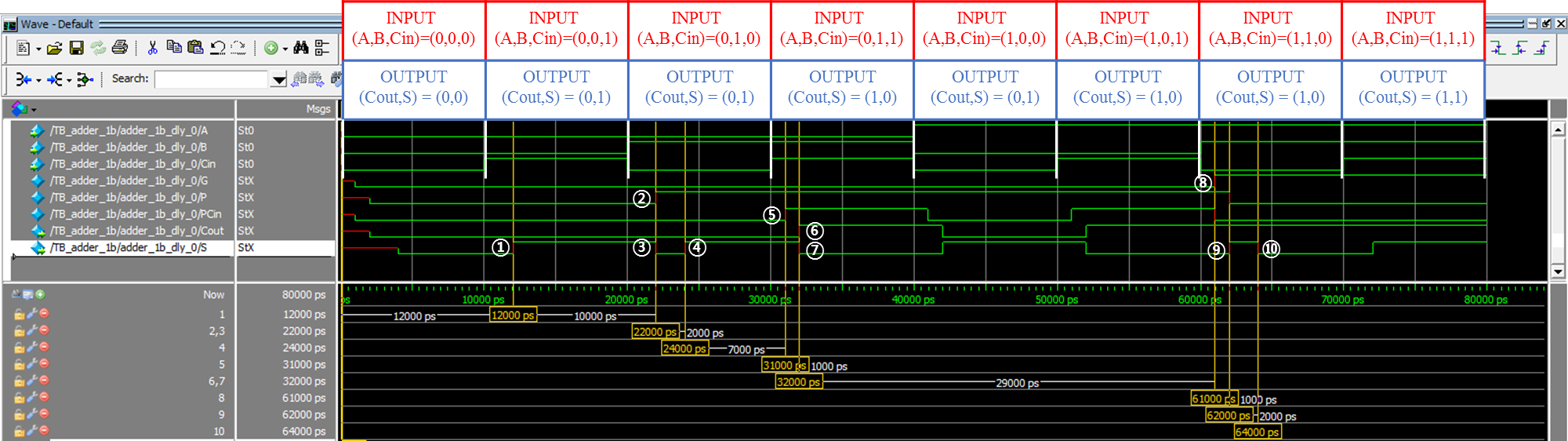


2) Coding of Testbench (1-bit Adder)

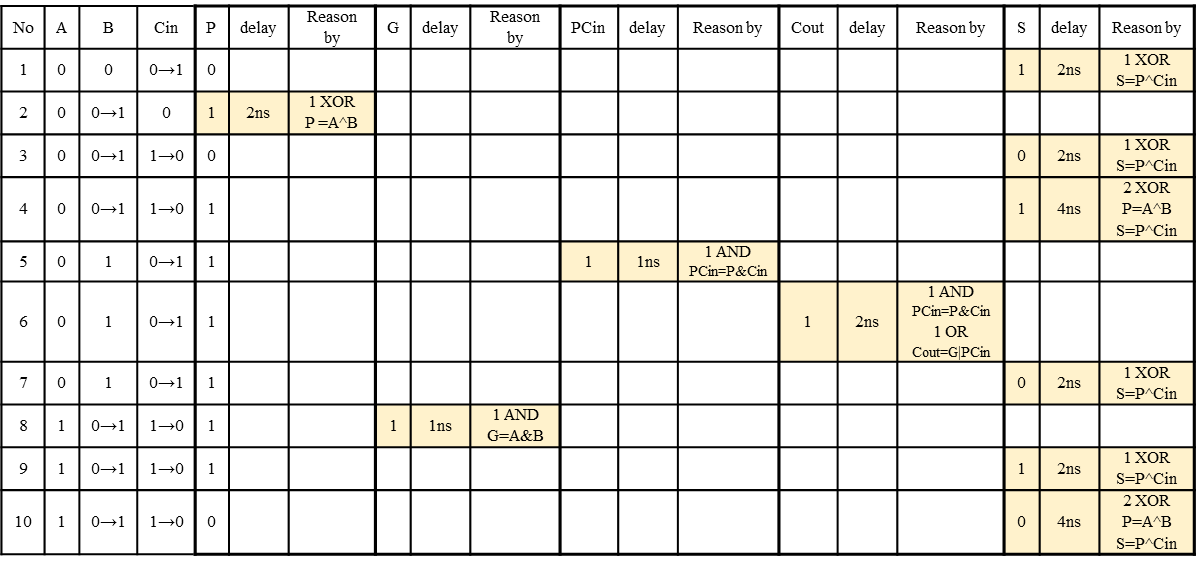


3) Simulation result in waveform

Problem. 3-1) Generate the waveform using the DUT and the Testbench



Problem. 3-2) Fill out the yellow colored cells (delay compared to the no gate delay circuit of the table below and its reason) like examples.



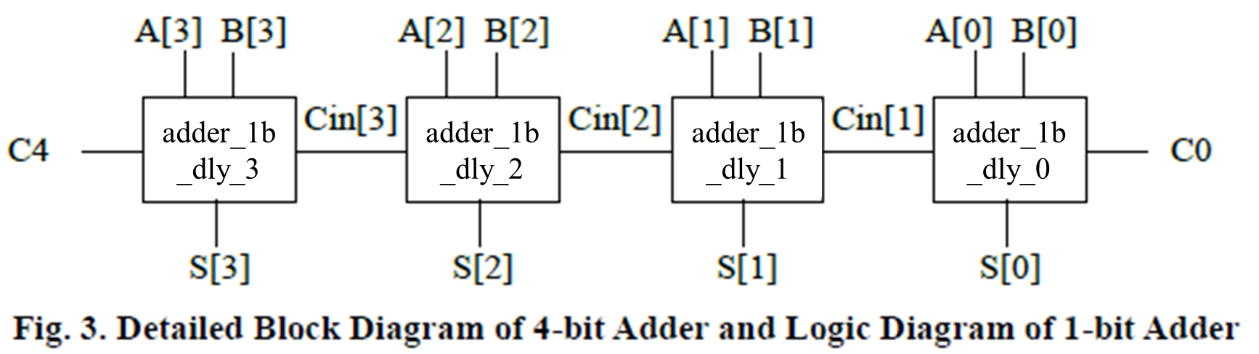
**3. Evaluation of the simulation result**

By reviewing the above waveform, it is possible to verify that according to all the combinations of input (A,B,Cin), corresponding results (S,Cout) are generated as exactly as the truth table with correct delay results

Accordingly, the simulation is done correctly.

**Part II. Design and Simulation of 4-bit Ripple-Carry Adder with gate delay**

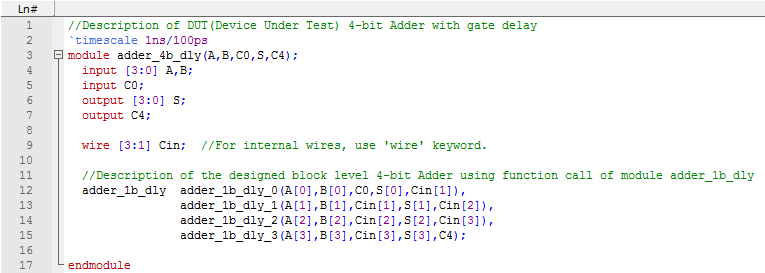
**1. Design of the required logic circuit to verify the simulation result**



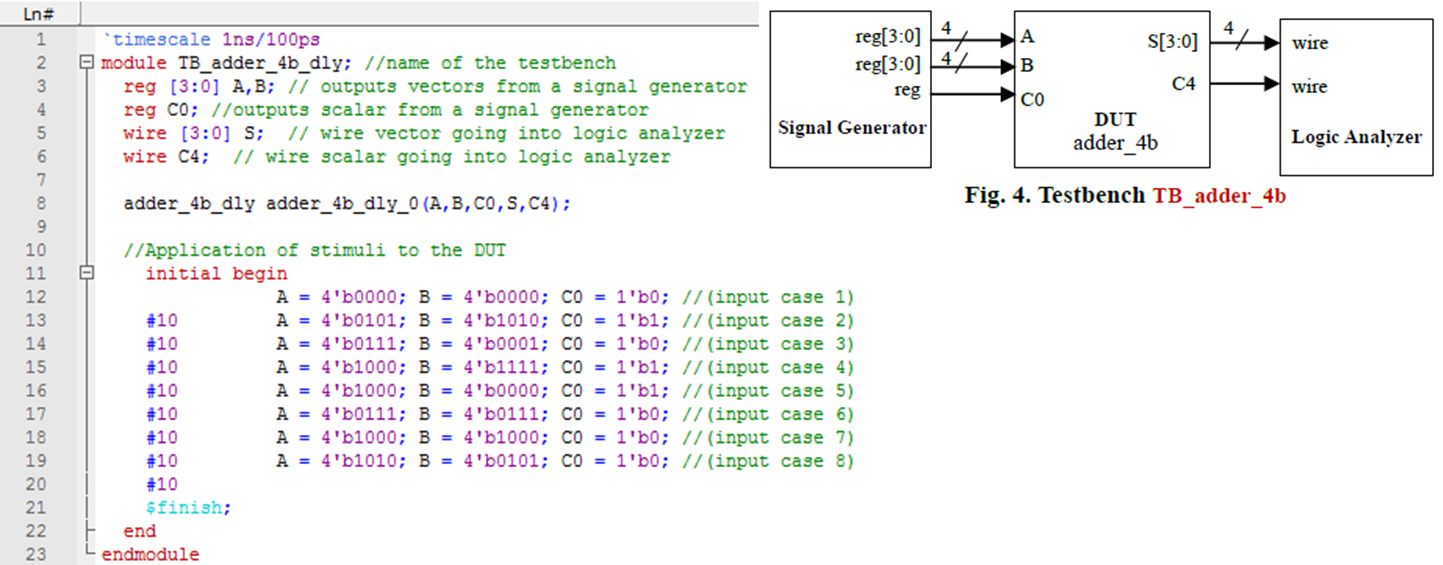
**2. Simulation**

1) Coding of DUT (4-bit Adder)

(Declare in the first line of the module `timescale 1ns/100ps).

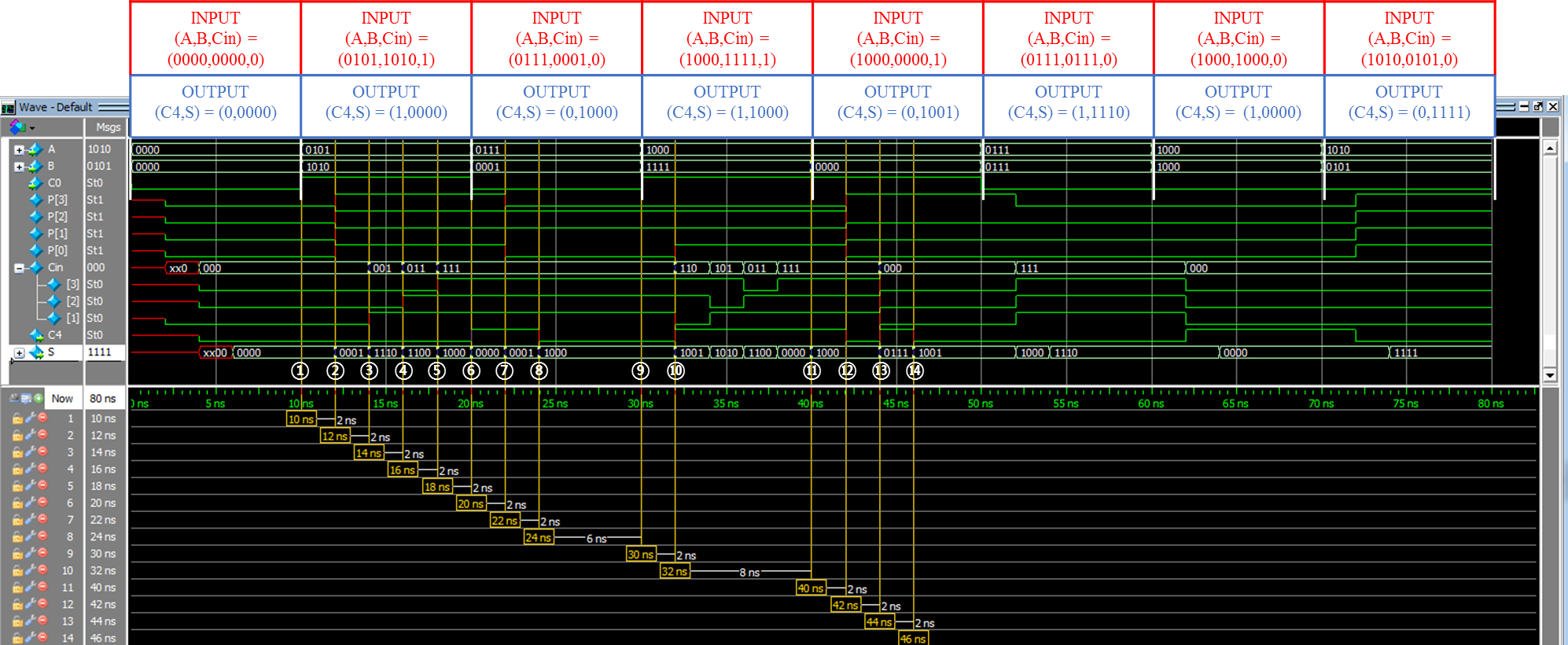


2) Coding of Testbench (4-bit Adder)

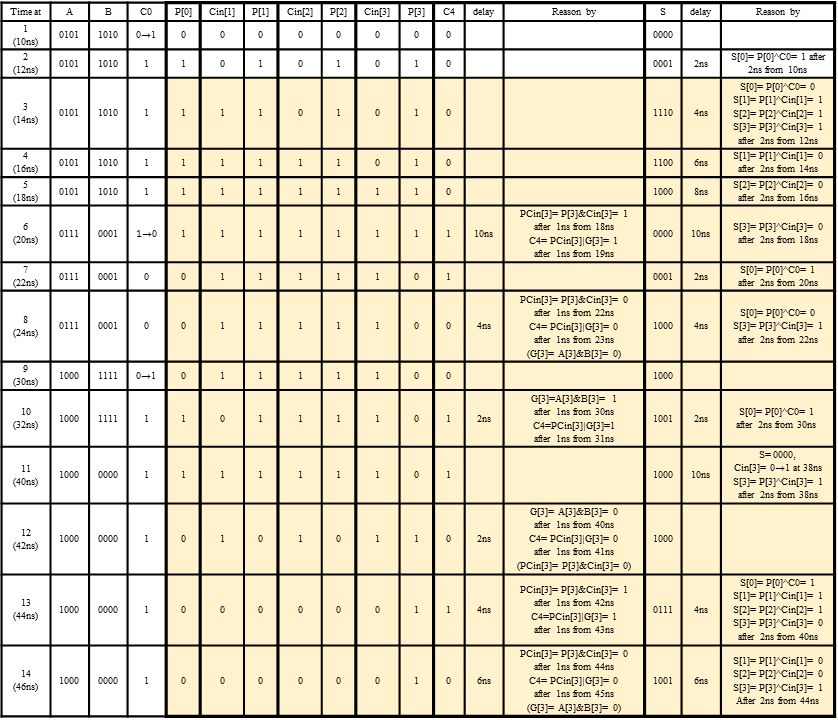


3) Simulation result in waveform

Problem. 3-1) Generate the waveform below using the DUT and the testbench.



Problem. 3-2) Fill out the yellow colored cells like examples.

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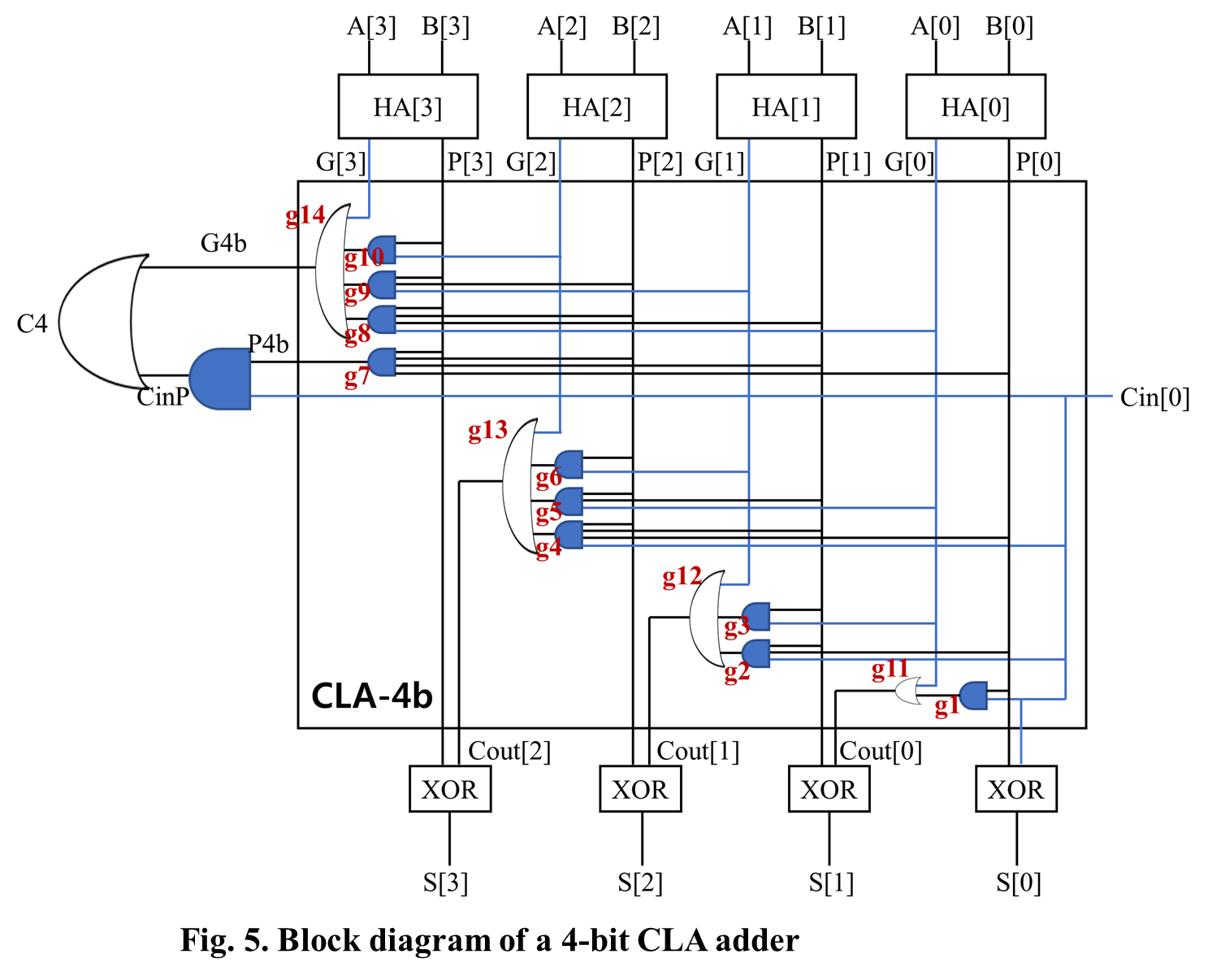
**3. Evaluation of the simulation result**

By reviewing the above waveform, it is possible to verify that according to some typical combinations of 4-bit inputs (A,B) with Carry-in C0, corresponding 4-bit addition results (S) with Carry-out, C4, are generated as exactly as the manual calculation result considering each gate delay.

Accordingly, the simulation is done correctly.

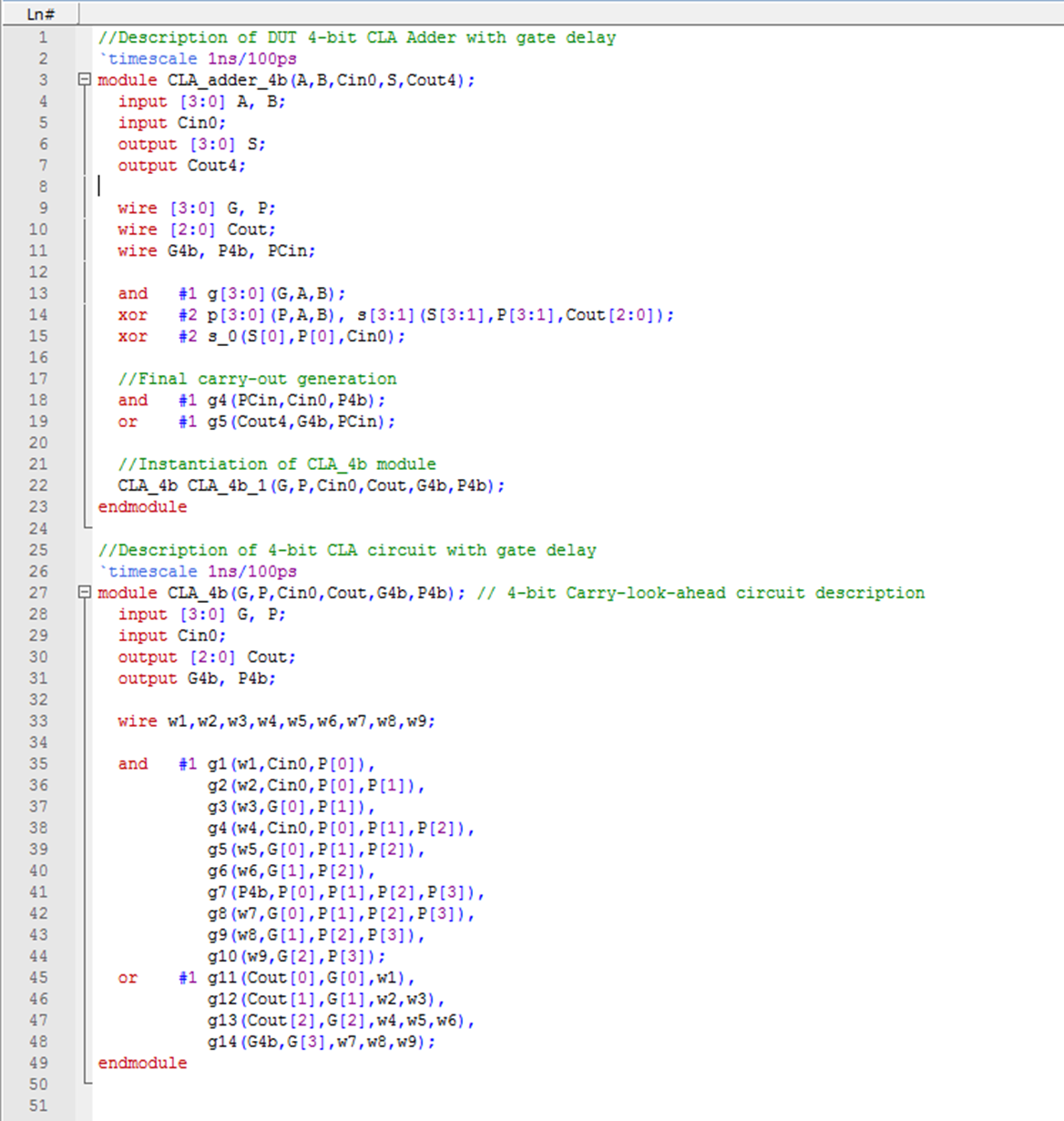
**Part III. Design and Simulation of 4-bit Ripple-Carry Adder with gate delay**

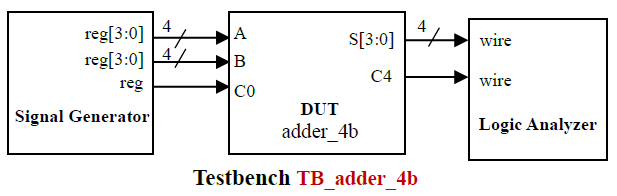
**1. Design of the required logic circuit to verify the simulation result**

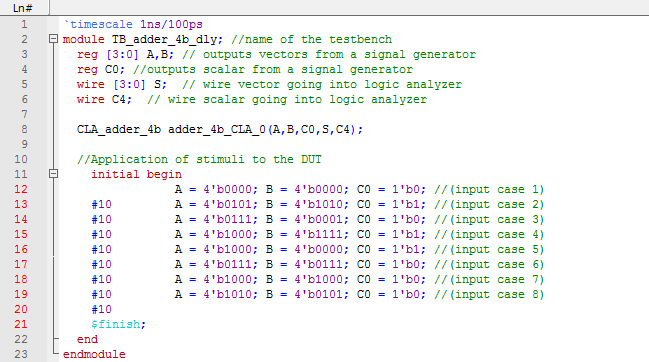
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**2. Simulation**

1) Coding of DUT (4-bit CLA Adder)

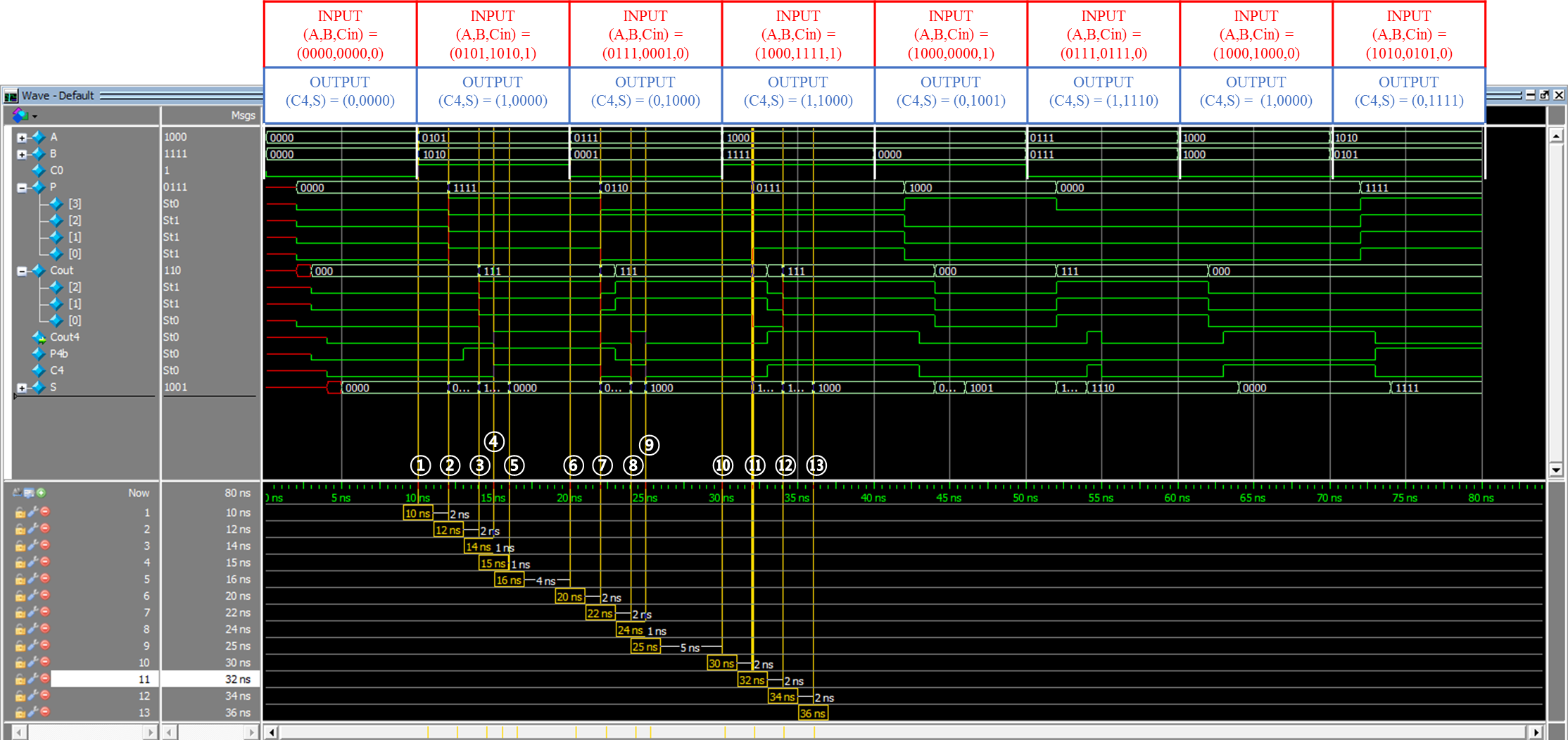


 2) Coding of Testbench (4-bit CLA Adder)

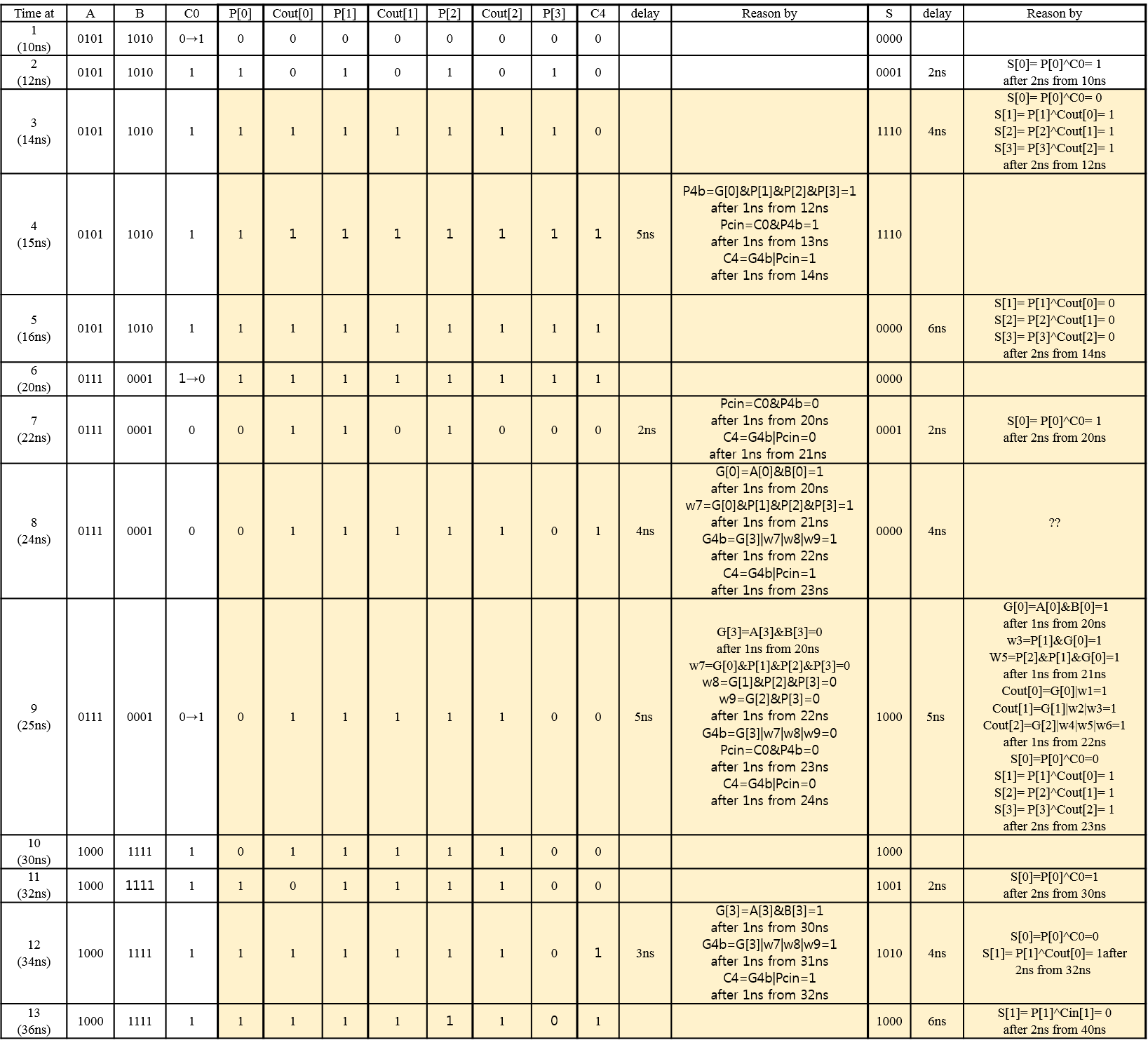


3) Simulation result in waveform

Problem. 3-1) Generate the waveform below using the DUT and the testbench.



Problem. 3-2) Fill out the yellow colored cells like examples.

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**3. Evaluation of the simulation result**

By reviewing the above waveform, it is possible to verify that according to some typical combinations of 4-bit inputs (A,B) with Carry-in C0, corresponding 4-bit addition results (S) with Carry-out, C4, are generated as exactly as the manual calculation result.

Accordingly, the simulation is done correctly.